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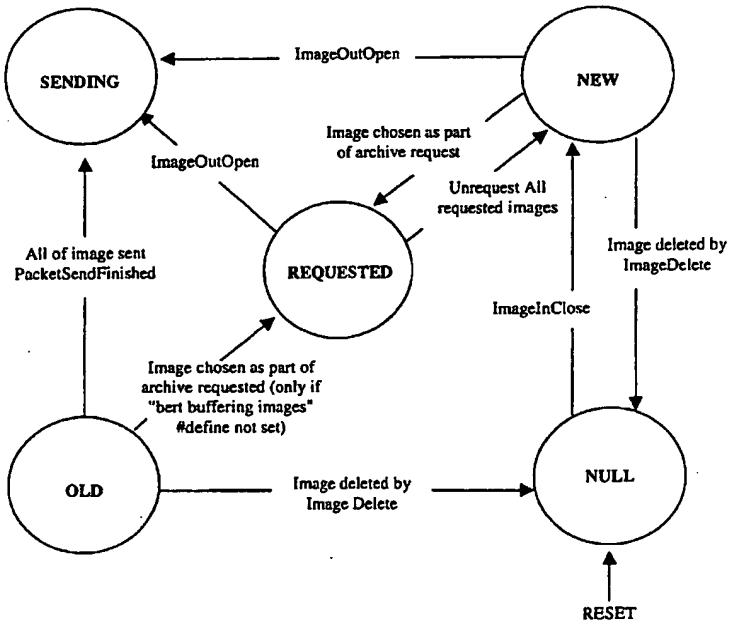

(57) Abstract

The present invention relates to a data capture device which inclcudes a data capture means, and a data output, and the data capture device characterised in that it includes processing means that to process the captured data into a format suitable for communication through the data output.

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IMPROVEMENTS IN OR RELATING TO CONTROL AND/OR MONITORING SYSTEMS

This invention relates to improvements in or relating to control and/or monitoring systems.

Reference around the specification should be made to the present invention in relation to security systems which are in fact control and/or monitoring systems.

BACKGROUND ART

An increasing number of security systems are being installed world-wide. Further, existing security systems are continually being upgraded as technology becomes smarter, more monitoring/control devices are available, and the desire for increased security increases.

Most complexes into which the systems are installed have existing communications networks. These networks all have various constraints which may include cabling, data transmission, processing and storage.

Each time a peripheral device for a security system is added to the communications network, a number of tasks maybe required to enable this to happen. These may include

- Adding additional software to the server of the communications network to process/translate the data entering the network from the peripheral.
- Adding extra cabling to connect the peripheral to the local area network or directly to the server.

- Upgrading the cabling of the local area network to accommodate increased rates of data transmission.
- Increasing the memory of the server in order to store additional data.
- Increasing the processing power of the server to handle the extra data.

To implement any of the above is expensive and time consuming. Further, implementation can lead to worker's downtime and possible security risks as the system is being taken offline to accommodate the changes being made.

Another problem associated with security systems is that the persons monitoring the system are exposed to a considerable volume of information. This can include a multiplicity of screens which must continually be monitored effectively. What can occur is an information overload when the person watching cannot continually assimilate all of the information in a manner that facilitates an efficient or effective monitoring function. Thus, it is possible that "alarm" and "unusual" situations can appear on the screens but not be seen or be acted upon as quickly as desired.

Another problem with security systems that utilise existing communications architecture is that the system may become inoperative, for example the server may "crash".

Thus, the security system can be dependant upon an unreliable communications network and disabled along with it. In some situations, it maybe that parties wishing to breach security will target this network.

Given the foregoing, will obviously desirable to have a system which is not necessarily dependent upon the existing communications network system to operate.

It is object of the present invention to address the above problems, at least to provide the consumer with the useful choice.

Further objects of the present invention will now become apparent from the following description which is given by way of example only.

DISCLOSURE OF INVENTION

According to one aspect of the present invention there is provided a data capture device which includes a data capture means, and

a data output,

the data capture device characterised in that it includes

a processing means that to process the captured data into a format suitable for communication through the data output.

According to other aspects of the present there is provided a monitoring system which includes at least one data capture device as described above.

According to a further aspect of the present invention there is provided a method of operating a data capture device characterised by the steps of:

a) capturing data, and

b) processing the data to a format suitable for communication to another component in a monitoring system, and

c) outputting the processed data

Reference for the majority of the specification will be made to the data capture device as being a digital video camera (DVC). It should be appreciated however that the principles of the present invention may apply to other data capture devices, for example a digital audio device such as an intercom.

In preferred embodiments of the present invention, the camera may include a memory or storage device to record selected data. This has a number of advantages.

One advantage is that if the main communication network crashes, data can be held within the camera to be accessed when the network is running again.

In preferred embodiments the camera is configured so it is capable of operating independently of the servers on the communications network. This independent configuration may include separate power supplies, separate processing and memory devices.

The selected data maybe any data that is useful in terms of the security system.

For example, the data may be the last information received over a certain time period. There may be a continual memory loop with old data being written over by new data.

Selected data may in some embodiments be a record of certain events which meet certain selection criteria and happened over a period of time.

For example, any event or alarm (of logical combination of events of alarms) may trigger the storage of appropriate data (whether visual, audio or otherwise).

Examples of typical events are:

- The person being granted access at a door with a card reader;
- The person being denied access at a door with a card reader;
- The contact on a reed switch opening to indicate that a door has opened;
- The contact on a reed switch opening to indicate that a window has opened;
- The motion detected by a camera;
- The motion detected by a passive infra-red (PIR) detector;
- A glass break detector detecting a glass break;
- A person speaking into an intercom.

An alarm is a type of event that is deemed to be out of the normal. A controller may have part of its processing capability, information to allow it to determine whether an event is an alarm based on the following criteria;

- The source of the event (e.g. from which peripheral device the event was detected).
- The type of the event (e.g. contact open or contact closed)

- The time and date (e.g. a certain event is only alarmed outside normal working hours).
- Whether the source and type of event is a group of alarm points that is currently armed or

With regard to alarm points, the group may correspond to a geographical grouping (specific area or building) or be part of a logical grouping (e.g. or the reed switches monitoring windows from the outside of a building). These group of alarm points maybe armed or disarmed manually (e.g. from a card reader operator workstation PC automatically) when the area that the alarm points monitors occupied or unoccupied or automatically by time and day. An alarm point in the group of alarm points only creates an alarm when the group of alarm points as a whole is armed.

Thus it can be seen that if the present invention has a memory device which hold data coming in over certain time period, it is then possible that once an alarm or an event is detected, data relating immediately before the event as well as during after can be held "stored".

It should be appreciated that this is an important feature in a security system and can offer valuable information about the events surrounding a breach of security.

According to one aspect the present invention, the DVC has integrated intelligence such that the camera itself can effect data processing. Data processing is thus performed on captured images at the camera thereby enabling the camera to rapidly analyse image data and perform functions which can include motion

detection, motion detection within a region of the camera's field of view, false detection recognition (i.e. curtains moving in a breeze) and tracking objects to record the path of movement through the field of view (useful for detecting access to an area in the camera's field of view in authorised and unauthorised directions.

In its simplest application the DVC can be used both as a surveillance camera and as a replacement for a standard passive infra-red motion detector. When performing motion detection the camera will be able to generate an event to be logged by the system host in the same manner as a contact alarm for a traditional passive infra-red detector. Under software control from an operator work-station the DVC can provide images on screen with the operator being able to select any camera in the system.

By virtue of its "intelligence" the DVC can analyse images captured and be able to process the images for subsequent transmission to the host system or storage for later transmission of any images arising from motion detection, false detection or tracking objects. To indicate an unusual or alarm situation the camera can immediately on-pass such information to the host system for analysis at the operator work-station. In this manner, the camera can distinguish between routine information and alarm/unusual situation information thereby resulting in the operator work-station only being provided with information on which immediate analysis/action is required. This reduces information overload on the operator. An alarm function can be included to alert the operator to the alarm/unusual situation so as to ensure that the images transmitted from the digital camera are immediately analysed.

In some embodiments of the present invention, the camera may include the ability to indelibly stamp images with a digital "watermark" to authenticate images. Preferably, the watermarking is sufficiently tamper proof that it would be able to be used as court evidence. For example, the watermarking may be used in connection with an image linked to an event such that the watermark can identify which camera (in its system) captured the image, the date and time the image was captured and verify that the image had not been tampered with in any way since it was captured.

In one embodiment of the present invention, the watermarking is carried out in two stages. First, a digital signature of various data relating to the image is calculated. Secondly, part of this digital signature is used as a bit-pattern that is embedded in the quantised wavelet co-efficient output stream.

In preferred embodiments of the present invention, the data that is received by the camera is also compressed before transmission to the security system.

In typical image compression techniques, often only the change in data is transmitted. For example, there may be a scene in which something moves. Standard compression techniques would send one image having the full scene and in subsequent images of only the moving object as this is the only part of the image which has changed.

The applicant has recognised that this form of image compression is not suitable for security systems. In security systems, it is desirable to have stand alone frames which are independent of each other. This means that to tamper with the images,

each frame will have to be tampered with which is difficult to do so. Thus, this aspect of the present invention gives greater veracity of data.

If it can be seen that the ability to compress the data means that a smaller communications band-width can be used, and it is easier to provide data buffers to cope with the information.

The present invention offers a number of advantages over the prior art. There is provided a digital video camera that has integrated intelligence.

Image data can at least be partially processed on board the current camera such as priority data (e.g. alarm or an unusual situation) is determined at the camera and stored and transmitted to the front end of the monitoring system.

Likewise, similar advantages are possible with a digital audio device such as an intercom.

The present invention also provides a monitoring system in which data can be processed at the surveillance camera which prevents "information overload" at the front end of the system.

As with the visual digital camera, the digital intercom can also process data in a similar way, for example with compression techniques, and event bracketing provided by having a buffer system that allows data to be stored before, during and after an event and so forth.

Communication of selected data reduces the information of the load that the conventional operators can be subject to. It also reduces the requirement for large band-width communication between the camera and the monitoring system.

BRIEF DESCRIPTION OF DRAWINGS

Aspects of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram illustrating basic functional blocks of a digital video camera in accordance with one embodying present invention and,

Figure 2 is another schematic diagram indicating the workings of a digital video camera in accordance with one embodiment present invention and,

Figure 3 is a schematic view of memory allocation in accordance with one embodiment of the present invention and,

Figure 4 shows the transitions of the image states and functions that cause them in accordance with one embodiment of the present invention.

BEST MODES OF PRESENT INVENTION

Referring firstly to Figure 1 of the drawings the DVC consists of six basic functional blocks as shown. The communications block 10 is in the system being described herein the CARDAX™ Local BUS interface for the camera. As will be appreciated by those skilled in the art galvanic isolation can be provided between the camera electronics and the Local BUS communication lines which can also be provided with protective devices.

The communications block 10 is based around a microprocessor with various integrated peripherals including parallel and serial ports. The microprocessor is provided with FLASH E^2 PROM non-volatile memory to hold programme code and set-up data and volatile SRAM memory for general use.

The non volatile memory holds programme code and set-up data for both the communications block 10 and the main processing block 11. The communications block 10 down-loads main programme code and set-up data as required (for example, at power-up reset) to the main processing block 11 which is provided only with volatile memory for data and programme control. In normal operation programme code and set-up data can be updated/down-loaded from an external device via the Local BUS interface. Several different versions of programme code and set-up data for both the communications block 10 and the main processing block 11 may be stored in the non-volatile memory. Software control mechanisms select the version(s) to be used in any particular time.

The communications block 10 can also provide unit address initialisation, unique electronic serial number identification, tamper detection, micro-controller supervisory functions, and visual processing indications using LEDs.

The main processing block 11 is based around a digital signal processor ("dsp"). The dsp is provided with SRAM which it can flexibly segment into areas of data and programme code memory. The dsp primarily analyses images and compresses data.

A multi-functional "host port" associated with the dsp in processing block 11 connects to the address and data BUS system of the communications block 10 to

provide a high-speed bi-directional, parallel data transfer link between the two functional blocks. The dsp appears to the microprocessor in the communications block 10 as a local peripheral in its 1/0 map.

An image capture block 12 is based around a CMOS active pixel sensor (APS) imaging chip which is effectively a camera-on-a-chip and the necessary bias circuitry for it. The image capture block 12 acquires images and presents them as a stream of digital data, on an 8-bit wide data BUS to the video buffer block 13. An image from the video buffer block can vary in size, e.g. it can be a full frame or a window (rectangular block) from within the full frame.

Infra-red LEDs can be included in the image capture block 12 to provide infra-red illumination. The DVC can, therefore, monitor either in the visual light spectrum or in the infra-red spectrum and a wide variety of ambient lighting condition.

The video buffer block 13 consists of SRAM for storing image data acquired by the image capture block 12. While another image is being accumulated in the image capture block 12, the main processing block 11 has access to the data stored in the video buffer block 13.

A set of BUS transceivers interface the SRAM in the video buffer block 13 to the 8-bit data BUS system of the image capture block 12 and another set of BUS transceivers interface the SRAM to the 24-bit data BUS system of the main processing block 11. Through the transceivers, dual port access to the SRAM is provided but only one "port" can be accessed at a time. The APS in the image capture block can effectively write 8-bit data into the SRAM of the video buffer block 13.

The dsp can effectively read data from and write data to the SRAM of the video buffer block 13 as 24-bit words.

Image data from the image capture block 12 is passed to the video buffer block 13, 1-BYTE (8-bit) at a time. As each BYTE is passed over it is loaded into one of three BUS transceivers such that every three consecutive BYTES are loaded to effectively form a 3-BYTE (24-bit) word. When 3 BYTES have accumulated in the BUS transceivers they are simultaneously latched to the transceiver outputs and then written into the SRAM as a single 24-bit word.

A sensor/buffer control block 14 consists of a small microprocessor and various discrete logic. Much of the discrete logic is in a programmable logic device (pld). A full-duplex, asynchronous serial link between the dsp and the image capture microprocessor results in the dsp being able to request a variety of options that the microprocessor in the image capture or sensor/buffer control block 14 and the APS are able to provide. The infra-red LEDs are controlled from the microprocessor in the control block 14. The microprocessor in block 14 communicates with the sensor over an I^2C BUS synchronous serial link.

The power supply block 15 takes power from an external source and generates all the necessary power rails for the DVC electronics. Line protection and filter circuitry are included.

In a preferred form of the invention as herein described the following power rails are generated:-

5V for digital circuits in the communications block 10 and image capture block 12;

5V for analogue circuits in the image capture block 12;

5V programming supply for the non-volatile memory in the communications block 10;

3.3V for digital circuits in the main processing, video buffer and sensor-buffer control blocks 11 and 14;

7-10V for the IR LEDs.

Typically, an image captured by the APS is transferred directly into the video buffer 13 via one BUS interface. The dsp then accesses this by another BUS interface and processes it. Compressed images can be stored until they are transferred from the main processing block 11 to the communications block 10 which can transmit them over the Local BUS or overwritten by newer images.

The electronics for the DVC resides on two multi-layer printed circuit board (pcb) assemblies. One is a small assembly consisting of the APS and the bias circuitry and oscillator associated with it, the lens for the APS and IR LEDs used for illumination in dark environments. All other electronics reside on the second larger pcb. The two assemblies are electrically inter-connected using a flexible pcb strip. The pcbs and lens assemblies are housed within a sealed plastic enclosure. A plastic mounting bracket preferably secures the small image capture pcb assembly to the larger pcb assembly in a manner that allows the APS, lens and

IR Leds to be rotated in one plane. This allows a degree of freedom of movement for the module to be aligned during installation.

According to a preferred form the mounting is such that it is possible to mount the DVC at any angle on (for example, but not restricted to) a wall, a ceiling, or an adjustable bracket that allows the camera to be easily pointed at an appropriate view. The standard combination of a wide-angle lens and having the image capture assembly internally mounted at a 45° angle means that in most cases the DVC can simply be placed at a location without any internal adjustment being required. In cases where internal adjustment of the image capture assembly is required, it can be rotated up to 45°.

Installing the DVC according to a preferred form involves a plastic mounting plate. The plate is affixed to a wall, ceiling, pan/tilt mount or other camera mount and provides terminals for attaching external wiring for power and Local BUS communications. These wires protrude through the centre of the mounting bracket which is fixed in place with screws. The main DVC enclosure is pushed onto the plastic plate and rotated until it is locked in place. This simultaneously connects the external power and communications terminals through to the electronics within the enclosure by using studs that wipe over a flexible portion of the terminals. A spring-like action ensures good contact between the terminals and the studs.

Throughout the DVC extensive use is made of two discrete logic families. The DVC uses two different supply rails for digital, electronics, namely, 3.3V and 5V. Because of this mixed supply arrangement one of the logic families must be able to interface between the different operating levels effectively.

One of the logic families used is a standard advance CMOS logic series, 74Acxxx. Such devices can be powered by either the 3.3V power rail or the 5V power rail but devices powered by the 3.3V rail cannot be driven by devices powered by the 5V rail. This family is selected as high speed logic is necessary in the DVC and only small propagation delays can be tolerated in many area. The 74Acxxx series is effective and is also readily available.

Another logic family used is the 74LCXxxx family which is specifically designed to be powered between 2.0V and 3.6V. These fast devices with small propagation delays have 5V tolerant inputs. Because the inputs can tolerate 5V signals these devices are particularly used where voltage level-conversion can be a problem.

To more fully describe the construction and operation of the DVC reference will now be made to the camera software operation and design.

As mentioned above, the DVC has three on-board microprocessors each of which performs a different function. While the same functionality could be achieved using one microprocessor this would complicate hardware and software design. As disclosed above, the three processors are a micro-controller in the image capture block 12, the dsp in the main processing block 11 and a micro-controller in the communications block 10 for communications and controlling the down-loadable code.

The major components of the image capture micro-controller PIC code are a frame controller and an asynchronous serial communications to I^2C communications converter.

Referring to Figure 2 the frame controller controls multiplexing of the image capture memory and banking of this memory.

Because the video memory can be accessed by the dsp 17 or the sensor 18 it is necessary to ensure that no accesses take place while the multiplexer 20 is switched to the wrong device. This is accomplished by using a token that is passed back and forth over the token interrupt lines 21 between the image capture controller 19 and the dsp 17. When the dsp 17 has the token the controller 19 switches the video memory to the dsp. When the dsp is finished with the imaging memory it returns the token to the controller 19. The controller 19 then waits until the next frame is due to be read out before switching the memory to the sensor 18. The sensor writes the frame and when it is finished the controller 19 sends the token back to the dsp.

The frame controller module on the controller 19 has several modes to put the image into the video memory in different ways. The first way (default) is to simply put the image into bank B1 all the time. The second mode puts the image into bank B2 all the time. The third alternates the image between the two banks B1 and B2. The final mode captures two images in quick succession and puts them into bank B1 and B2.

The frame controller functionality could be implemented entirely in hardware.

To enable access to all the functionality and configuration control registers of the image sensor 18 a serial communications link is employed. In the preferred form the serial communication standard and protocol used (inter-integrated circuit – I^2C) is not available as a hardware port on the dsp 17. To communicate with this

protocol it is necessary to implement the port in the software. This is achieved using the micro-controller of the image capture controller 19. The dsp communicates with the UART 22 of the controller 19 using standard asynchronous serial communications 23. The controller 19 takes the commands and data and passes them onto the image sensor 18. There are also commands from the dsp 17 to change settings and modes on the controller 19.

In an alternative arrangement the I^2C communications can be carried out directly from the dsp 17. This can be either a hardware I^2C port or a software implementation.

A sensor driver software module controls communications and interactions with the image capture controller 19 and the image sensor 18. The sensor driver software module has buffers for storing messages to go to the controller 19 and routines for processing messages returned. It also implements the sending and receiving of the video memory token.

The dsp code includes an image processing controller which acts as a wrapper for the image processing routines. Instead of calling the image processing routines directly when a new image is available (token received from controller 19) the image processing controller is called. The image processing controller is responsible for updating any information needed by the image processing routines, updating information that is needed for the image header, starting and stopping watchdog supervisory routines and sending the video memory token back to the image capture controller 19.

The storing of compressed images is an important feature of the DVC.

In most imaging systems analogue video or digital, the camera simply sends out the image information as it is collected. This means that communications must be of sufficient bandwidth to cope with full rate real time images. It also implies that there is some means of buffering the imaging at the other end of the chain for review.

As mentioned previously, the DVC includes memory set aside to store several tens of images. This means that the DVC can be capturing images without sending any out and have past history available on demand should it be needed. Because there is not a constant stream of imaging information coming out, a low bandwidth digital network can be used without fear of it being overloaded by imaging.

Unless adaptive, most lossy coders vary in performance with the complexity of the scene. All coder parameters being equal, a very complex scene (lots of detail) takes up more room than a less complex one. This means that the images stored in the DVC are assumed to be of variable length.

The requirements for image storage are:-

- Store as many images as is possible, delete them only when necessary.
- Be able to efficiently search the image buffer.
- Be able to send any of the stored images in any particular order.
- Images to be contiguous in memory to allow the use of DMA.
- Interface to put images in and read them out to be simple.

Figure 3 shows the organisation of the memory used for the image buffer. There is an array 28 of words which is statically declared. Space in array 28 is dynamically allocated to images as they are created. The images are indexed by an array of ponters 29 to image structures. The set of valid images are bounded by the oldest 0 to newest N images. These are indicated by pointers into the image pointer array 29. Both the image data array 28 and the image pointer array 29 are circular in nature. The wrapping around is handled by image buffer functions. Images cannot be allocated over the end of the image data array 28. If they run off the end, they are moved to the front and the free space 30 at the end is left vacant.

The images in the image data array are stored compressed in a large, statically allocated array of integers (words). There is a header on the front of every image with the following format:-

|Image Status |Size |Compression settings (3 words) |

Request number |Motion Status |Time Stamp| Data

Each of the header entries is one dsp word or 24-bits, except for the time stamp and compression settings. The image status is a state variable for a state machine that describes the behaviour of the image.

Figure 4 shows the transitions of the image states and the functions that cause them. There are two sets of functions that modify the image status. The functions for building the image and the functions for sending the image.

The image size is the number of words in the data field. The time stamp is 32-bit UNIX time followed by a 16-bit sequence number.

The dsp code includes a host port communications controller. The host port of the dsp 17 is a 24-bit to 8-bit asynchronous parallel interface. It appears mapped in the I/O space of the processor in the communications block 10 as a collection of 8-bit registers. There are three transmit and receive registers. These represent the high, middle and low bytes of a single dsp word.

The processor in the communications block 10 sends "host commands" to the dsp 17 by writing 8-bit values to a register. These commands trigger a vectored interrupt in the dsp 17. There are four services the microprocessor in the communications block 10 can request from the dsp, these are:-

- Request a Local BUS packet from the dsp.
- Request and internal packet from the dsp.
- Request the dsp to get ready to receive a Local BUS packet.
- Request the dsp to get ready to receive an internal packet.

The host port communications controller software module on the dsp uses the dsp's Direct Memory Access controller to send the data to the host port. This saves on core processing and BUS usage.

The DVC maintains a real time clock which is used to add a time stamp to the images as they are stored. This clock can be updated from the Local BUS.

The dsp code includes message buffering. In addition to sending out images over the host port the DVC also sends and receives other Local BUS and internal packets. The message buffering simply queues up the messages to be sent or the messages received until they can be sent or processed respectively.

Finally, the dsp includes as a major component supervisory routines. The DVC runs several supervisory routines.

There is a check for the integrity of the code, a check for the correct functioning of memory and three watchdog routines. The watchdog routines check for hanging of the image processing, the sensor communications and the frame capture. If any problems are detected they are reported to the Local BUS either directly if the dsp 17 is capable, or indirectly by a termination mode via the controller of the communications block 10.

Major parts of the code of the controller of the communications block 10 are a dsp controller, Local BUS port controller and supervisory routines.

The dsp controller controls all of the interfacing to the dsp17. It controls such things as the down-loading of code to the dsp, the hang supervision (watchdog) and the sending and receiving of packets from and to the dsp (including images).

The dsp code is downloaded to the dsp whenever the dsp is reset. The bootstrap code on the dsp waits for the length and address of the code to be sent to the host port and then captures the code.

The Local BUS port controller is a serial communications controller peripheral (SCC) built into the same chip as the microprocessor of the communications block

10. The SCC handles much of the low level detail of the Local BUS communications. The Local BUS controller code handles the higher level part of the Local BUS protocol and processes the messages destined for the communication block 10 microprocessor.

The dsp has no hardware watchdog for hang prevention. Instead, the microprocessor of the communications block 10 functions as a watchdog. The dsp must send interrupts to the microprocessor periodically. If the microprocessor goes for a certain time without receiving an interrupt from the dsp it assumes the dsp has hung. It then checks the host port for a termination code from the dsp and this is used to help determine what has gone wrong with the dsp.

The communications block microprocessor supervisory routines also run some self-monitoring of the code integrity and memory functionality.

Aspects of the present invention have been described by way of example only and it should be appreciated that modifications and additions may be made thereto without departing from examples from the scope of the appended claims.

THE CLAIMS DEFINING THE INVENTION ARE:

1. A data capture device which includes

a data capture means, and

a data output, and

the data capture device characterised in that it includes

processing means that to process the captured data into a format suitable for communication through the data output.

2. A data capture device as claimed in claim 1 wherein

the capture device is a peripheral device for use in a monitoring system, and

the data is processed into a format suitable for communication to another component in the monitoring system through the data output.

3. A data capture device as claimed in either claim 1 or claim 2 includes a memory device capable of recording selected data.

4. A data capture device as claimed in any one of claims 1 to 3 which is capable of communicating only selected data.

5. A data capture device as claimed in any one of claims 1 to 4 which includes the feature of alarm and event monitoring.

6. A data capture device as claimed in any one of claims 1 to 5 wherein the selected date recorded is the data immediately surrounding and including an event.

7. A data capture device as claimed any one of claims 1 to 6 in which processing means can compress the data captured.

8. A data capture device as claimed in any one of claims 1 to 7 wherein a data capture device is a digital video camera.

9. A data capture device as claimed in any one of claims 1 to 8 which adds a watermark to the image captured by the data capture device.

10. A data capture device as claimed in either claim 8 or claim 9 which includes the ability to detect motion.

11. A data capture device as claimed in any one of claims 8 to 10 which includes means to distinguish over false detection of motion.

12. A data capture device as claimed in any one of claims 8 to 11 which includes means to track objects record the path of movement through the field of view.

13. A data capture device as claimed in any one of claims 8 to 12 which includes infra-red motion detection.

14. A data capture device as claimed in any one of claims 8 to 13 which includes a wide angled lens and an image capture assembly fitted internally at approximately 45 degrees.

15. A data capture device as claimed in any one of claims 8 to 14 characterised in that the camera can be fixed into position by pushing and rotating the camera until it locks onto a mounting bracket which has electrical connections that connect to the camera once mounted.

16. A data capture device as claimed in any one of claims 1 to 6 which is a digital audio device.

17. A method of operating a data capture device characterised by the steps of:

a) capturing data, and

b) processing the data to a format suitable for communication to a component in a monitoring system, and

c) outputting the data processed data

18. A monitoring system which includes a data capture device as claimed in any one of claims 1 to 17.

19. A data capture device substantially as herein described with reference to and as illustrated by the accompanying drawings.

20. A monitoring system substantially as herein described with reference and as illustrated by the accompanying drawings.

21. A method substantially as herein described with reference to and as illustrated by the accompanying drawings.

Fig. 1

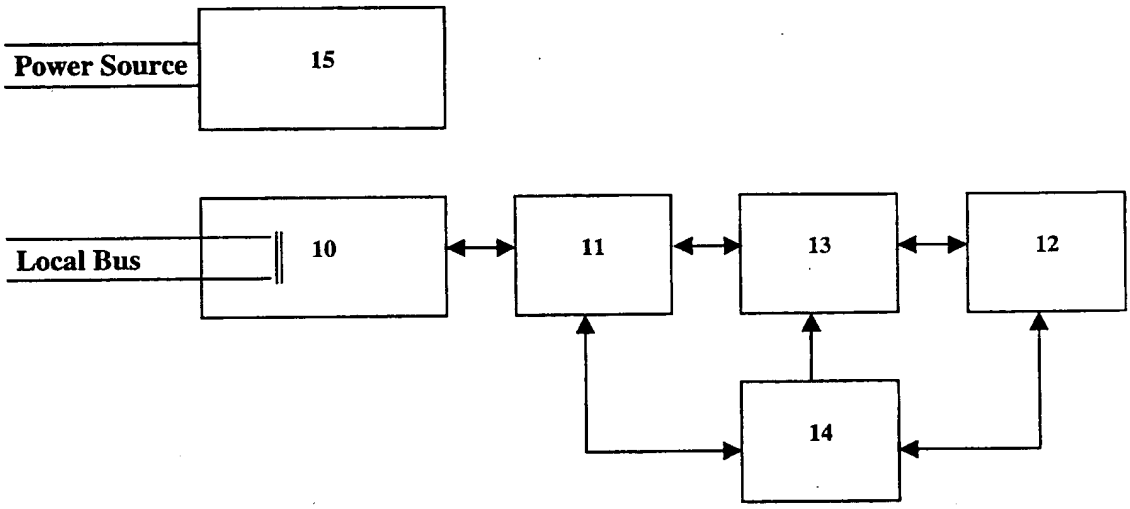


Fig. 2

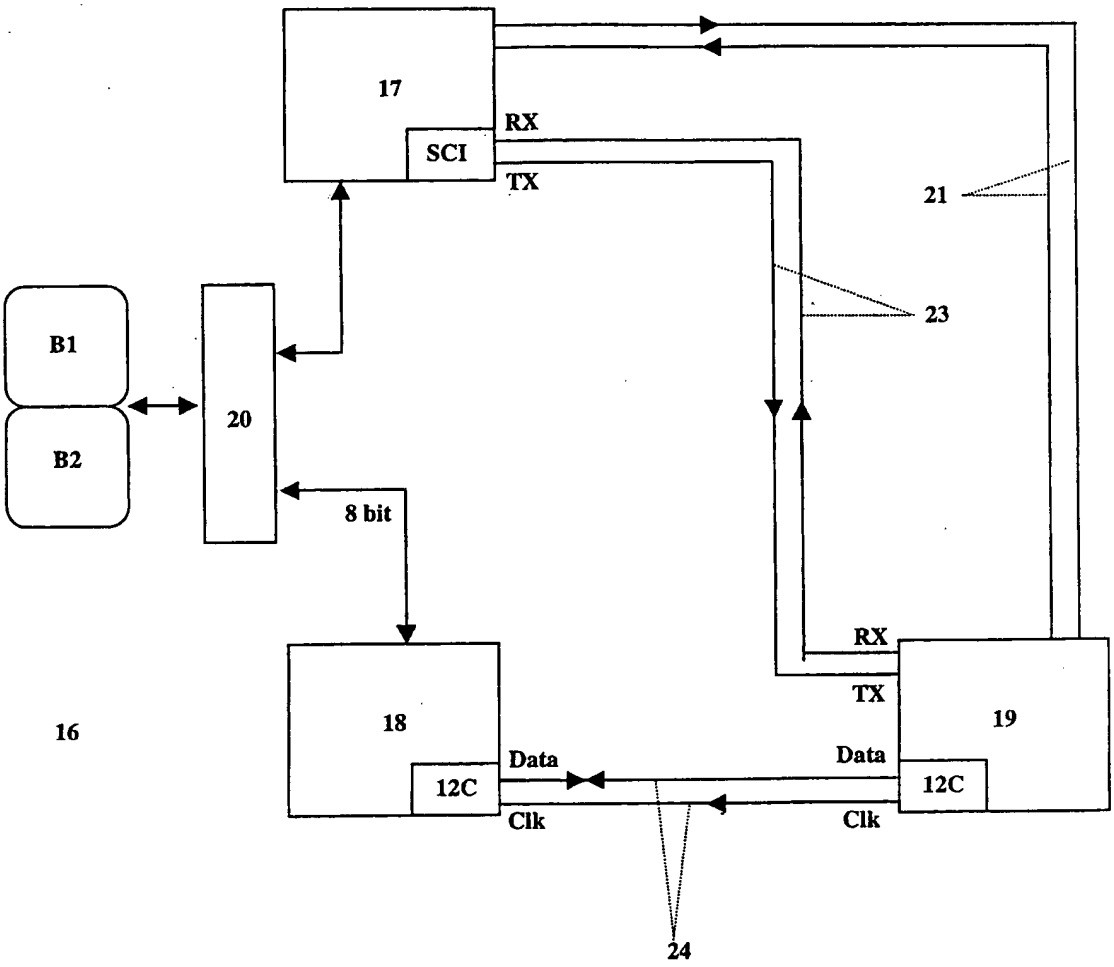

17
RX
SCI
TX
21
23
B1
B2
20
8 bit
RX
TX
16
18
19
Data
Data
12C
12C
Clk
Clk
24

Fig. 3

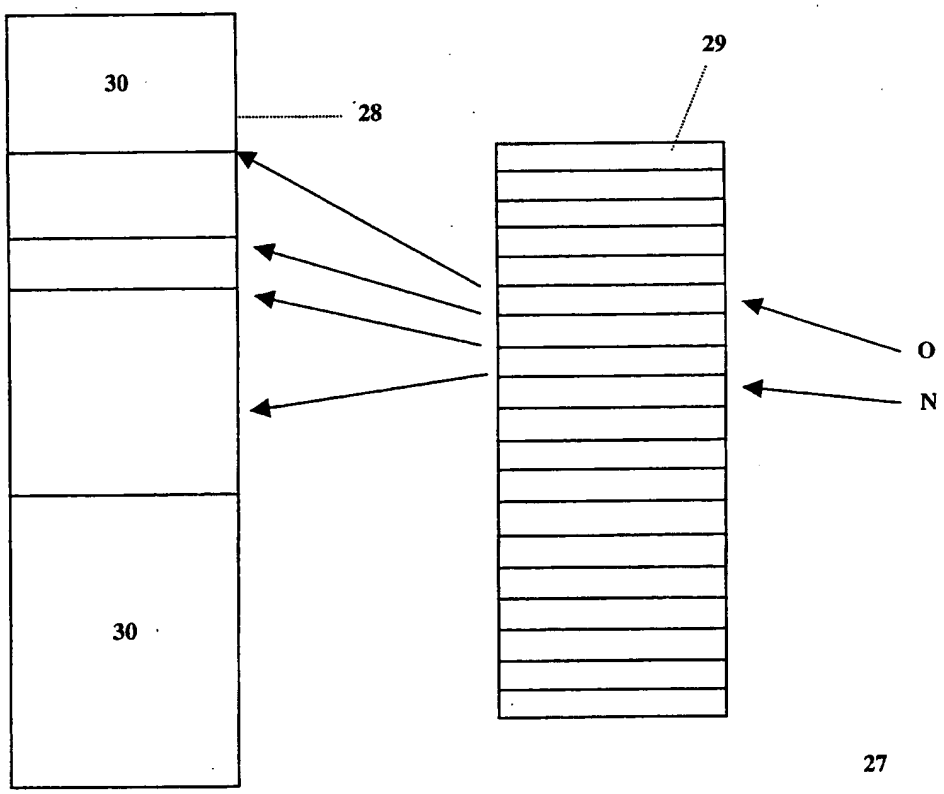
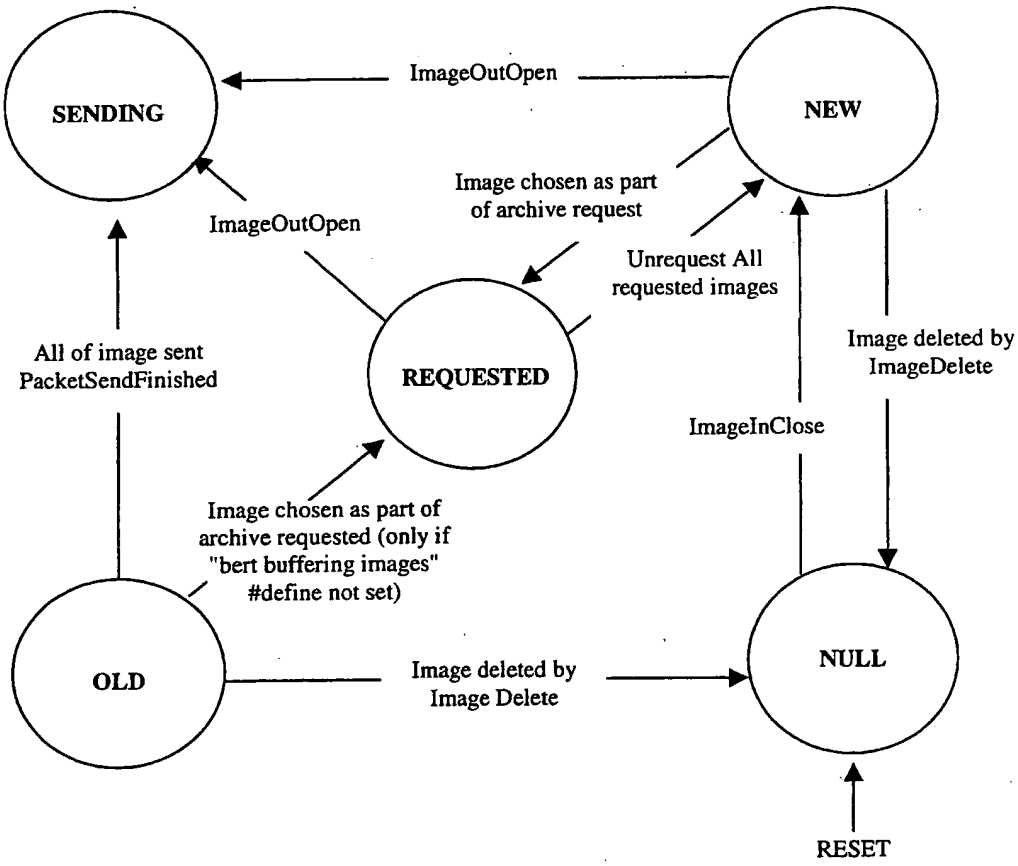


Fig. 4


SENDING
ImageOutOpen
NEW
Image chosen as part of archive request
ImageOutOpen
Unrequest All requested images
All of image sent PacketSendFinished
REQUESTED
Image deleted by ImageDelete
ImageInClose
Image chosen as part of archive requested (only if "bert buffering images" #define not set)
OLD
Image deleted by Image Delete
NULL
RESET

INTERNATIONAL SEARCH REPORT

national Application No
PCT/NZ 00/00011

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G08B15/00 G08B13/196

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G08B H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 689 357 A (HARRIS CORP) 27 December 1995 (1995-12-27)	1,2,4-8, 10-13, 17,18
Y	column 1, line 47 - line 55 column 2, line 14 - line 26 column 3, line 53 -column 4, line 5 column 4, line 50 - line 54	9
X	US 5 689 442 A (MOEN JERRY M ET AL) 18 November 1997 (1997-11-18) column 3, line 49 -column 4, line 17 column 4, line 46 - line 50	1-8, 16-18
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 May 2000	09/06/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De la Cruz Valera, D

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/NZ 00/00011

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 229 850 A (TOYOSHIMA KEIICHI) 20 July 1993 (1993-07-20)	1-7,17, 18
A	column 1, line 65 -column 2, line 32 column 5, line 42 - line 49 column 9, line 48	10,11,13

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